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# Design and Synthesis of Multiplier Using Dual Quality 4:2 Compressors with Higher Speed and Lower Power Consumption

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**Abstract:** In this paper, we have a tendency to propose four 4:2 compressors, which have the flexibility of change between the Exact and Approximate operative modes. Within the approximate mode, these dual-quality compressors offer higher speeds and lower power consumptions at the value of lower accuracy. Each of those compressors has its own level of accuracy within the approximate mode also as completely different delays and power dissipations in the approximate and actual modes. Exploitation of these compressors in the structures of parallel multipliers provides configurable multipliers whose accuracies (as well as their powers and speeds) may change dynamically throughout the runtime. The efficiencies of these compressors in a very 32-bit Dadda number are evaluated in a 45-nm CMOS technology by comparison their parameters with those of the approximate multipliers. The results of comparison indicate, on average, 46% and 68% lower delay and power consumption within the approximate mode. Also, the effectiveness of those compressors is assessed in some image process applications.

**Index Terms -** Accuracy, Approximate computing, Delay, Power. 4:2 compressors, configurable

## 1. INTRODUCTION

Parallel multipliers are utilized in superior applications wherever their large power consumptions could produce hot-spot locations on the die [3]. Since the power consumption and speed are crucial parameters within the style of digital circuits, the optimizations of these parameters for multipliers become critically vital. Very often, the improvement of one parameter is performed considering a constraint for the opposite parameter. Specifically, achieving the specified performance (speed) considering the limited power budget of transportable systems is difficult task. In addition, having a given level of reliability may be another obstacle in reaching the system target performance.

To meet the power and speed specifications, a variety of strategies at totally different style abstraction levels are suggested. Approximate computing approaches are supported achieving the target specifications at the value of reducing the computation accuracy [4].The approach is also used for applications wherever there's not a singular answer and/or a group of answers close to the correct result are often thought-about acceptable [5]. These applications include multimedia system process, machine learning, signal process, and different error resilient computations. Approximate arithmetic units are primarily primarily based on the simplification of the arithmetic units circuits [6]. There are several previous works that specialize in approximate multipliers which give higher speeds and lower power consumptions at the value of lower accuracies. Almost, all of the projected approximate multipliers are primarily based on having a set level of accuracy throughout the runtime. The runtime accuracy re configurability, however, is taken into account as a helpful feature for providing totally different levels of quality of service throughout the system operation [6]–[8]. Here, by reducing the standard (accuracy), the delay and/or power consumption of the unit is also reduced. Additionally, some digital systems, like general purpose processors, are also utilized for each approximate and precise (Exact) computation modes [4].

An approach for achieving this feature is to use an approximate unit along side a corresponding correction unit. The correction unit, however, will increase the delay, power, and space overhead of the circuit. Also, the error correction procedure could need more than one clock cycle (see [9]), that might, in turn, slow down the process additional. In this paper, we have a tendency to propose four dual-quality reconfigurable approximate 4:2 compressors, which give the flexibility of switching between the precise (Exact) and approximate operative modes during the runtime. The compressors are also utilized within the architectures of dynamic quality configurable parallel multipliers. The fundamental structures of the projected compressors consist of 2 components of approximate and supplementary. In the approximate mode, solely the approximate half is active whereas in the actual operative mode, the supplementary half along side some parts of the approximate half is invoked. The rest of this paper is organized as follows. In Section II, some previous works on the approximate

multipliers are reviewed. The internal structures of the projected dual-quality 4:2 compressors (DQ4:2Cs) are explained in Section-III. Section IV evaluates the accuracy of the Dadda utilizing the projected compressors whereas the effectiveness of the projected compressors is assessed in Section V. Finally, this paper is complete in Section VI.

## 2. LITERATURE SURVEY

While there are several works in coming up with approximate multipliers, the analysis efforts on accuracy configurable approximate multipliers are restricted. During this section, we review some of these works. In [10], a static section methodology (SSM) is given, that performs the multiplication operation on an m-bit section ranging from the leading one little bit of the input operands wherever m is adequate to or bigger than n/2.Hence, an m × m multiplier consumes a lot of less energy than other multiplier. Also, a dynamic vary un biased multiplier (DRUM) multiplier, that selects an m-bit section, starting from the leading one little bit of the input operands, and sets the least important little bit of the truncated values to "1," has been proposed in [11]. During this structure, the truncated values are multiplied and shifted to the left to come up with the ultimate output. Although, by exploiting smaller values for m, the structure of [11] provides higher accuracy styles than those of [10], its approach needs utilizing additional complicated electronic equipment.

A bio inspired approximate multiplier, referred to as broken array multiplier has been projected in [13]. During this structure, some carry save adder cells, in each vertical and horizontal direction during the summation of the partial product, have been omitted to avoid wasting the ability and space and scale back the delay. In [14], 2 approximate 4:2 compressors are projected and utilized in Dadda multiplier. The projected compressors only operated within the approximate mode. In [1], by modifying the Karnaugh map of a two × two multiplier , AN approximate two×two multiplier with a simpler structure has been projected. An inaccurate multiplier style strategy supported redesigning the multiplier into 2 multiplication and non-multiplication parts was introduced The multiplication half was constructed supported the traditional multipliers where as the non multiplication half was enforced in AN approximate structure with such as worth of error. It ought to be noted that each of the approaches given in [1] and [12] suffer from high relative errors.

In [15], a high accuracy approximate 4×4 Wallace tree multiplier was projected. This multiplier utilized a 4:2 approximate counter resulting in delay and power reductions of the partial product stage of the 4×4 Wallace tree. During this paper, the proposed little multiplier was wont to type larger multipliers. Due to the array structure of this approximate multiplier, its delay was giant. Additionally, an EDC unit was urged to be used at the output of the approximate four × four Wallace tree. The unit generated the precise output within the case of the exact operational mode. In [16], by proposing an approximate adder with a little carry propagation delay, the partial product reduction stage was sped up. During this paper, an OR-gate-based error reduction unit was additionally projected. In [17], a rounding based approximate multipliers (ROBA) has been projected that round the input operands into the closest exponent of 2. This way the multiplication operation became less complicated. It ought to be noticed that the error recovery unit (those in [1], [12], [15], and [16]) will increase the ability consumption and delay of the multiplier.

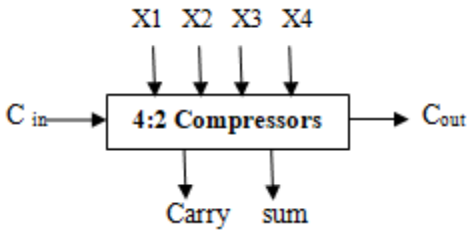


Fig.1. Block diagram of 4:2 compressor

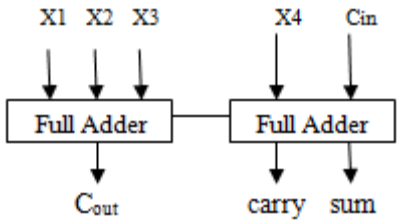


Fig. 2. Structure of the conventional 4:2 compressor

This means that accuracy configurable multipliers would have large delay and power overheads. In this paper, we propose compressors, which have the ability of switching between the approximate and exact modes with very small delay and power overheads.

## 3. PROPOSED 4:2 COMPRESSORS

In this section, first, the details of an exact compressor are discussed. Next, the overall structures and the details of the suggested dual-quality approximate compressors are described.

### *3.1 Exact 4:2 Compressor*

To reduce the delay of the partial product summation stage of parallel multipliers, 4:2 and 5:2 compressors are wide employed [18]. Some compressor structures, that are optimized for one or a lot of style parameters (e.g., delay, area, or power consumption), are planned [18], [19]. The focus of this paper is on approximate 4:2 compressors. First, some background on the precise 4:2 Compressors is conferred. This type of Compressors, shown schematically in Fig. 1,

has four inputs (x1–x4) along side associate inputs carry (Cin), and two outputs (sum associated carry) along side an output Cout. The internal structure of a definite 4:2 Compressors consists of 2 serially connected full adders, as shown in Fig. 2. In this structure, the weights of all the inputs and therefore the add output square measure constant whereas the weights of the carry and Cout outputs square measure one binary bit position higher. The outputs add, carry, and Cout square measure obtained from

$$sum = X1\text{^}X2\text{^}X3\text{^}X4\text{^}C_{in} \quad (1)$$

$$Carry = (X1\text{^}X2\text{^}X3\text{^}X4)*C_{in} + (X1\text{^}X2\text{^}X3\text{^}X4)*X4 \quad (2)$$

$$C_{out} = (X1\text{^}X2)*X3+(X1\text{^}X2)*X1 \quad (3)$$

### 3.2 Proposed Dual-Quality 4:2 Compressors

The proposed DQ4:2Cs operate in two accuracy modes of approximate and exact. The general block diagram of the compressors is shown in Fig. 3

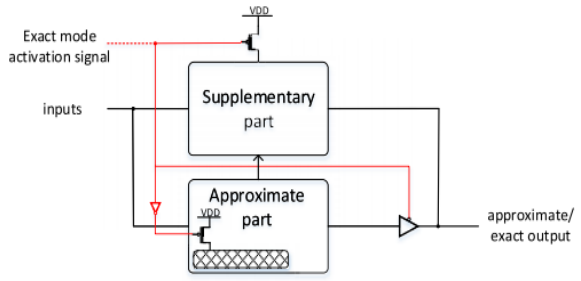
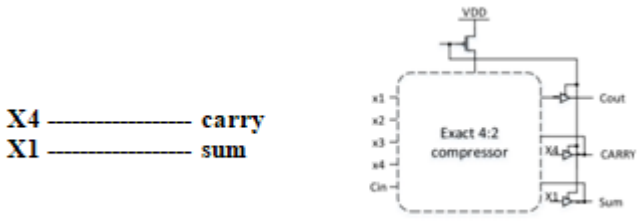



Fig .3. Block diagram of the proposed approximate 4:2 compressors

The hachured box in the approximate part indicates the components, which are not shared between this and supplementary parts.




(a) (b)

Fig.4. (a) Approximate part structure of DQ 4:2$C_1$ (b)Overall structure of DQ 4:2$C_1$

The diagram consists of two main components of approximate and supplementary. During the approximate mode, solely the approximate half is exploited while the supplementary half is power gated. During the exact in operation mode, the supplementary and a few components of the approximate components are utilized. Within the planned structure, to reduce the facility consumption and space, most of the components of the approximate half also are used through out the exact in operation mode. we have a tendency to use the facility gating technique to turn OFF the unused elements of the approximate half. Also note that, as is clear from Fig.3, within the precise in operation mode, tri-state buffers are utilized to disconnect the outputs of the approximate half from the first outputs. During this style, the shift between the approximate and precise in operation modes is quick. Thus, it provides us with the chance of designing parallel multipliers that are capable of shift between completely different accuracy levels throughout the runtime. Next, we discuss the main points of our four DQ4:2C's supported the diagram shown in Fig. 3. The structures have completely different accuracies, delays, power consumptions and space usages. Note that the ith planned structure is denoted by DQ4:2Ci. The basic idea behind suggesting the approximate compressors was to minimize the distinction (error) between the outputs of actual and approximate ones. Therefore, so as to settle on the correct approximate styles for the compressors, an in depth search was performed. Throughout the search, we have a tendency to used the reality table of the exact 4:2 Compressors because the reference.

(1)Dual Quality 4:2 compressor Structure 1 (DQ4:2C1):

For the approximate a part of the first projected DQ4:2C structure, as shown in Fig. 4(a), the approximate output carry (i.e., carry) is directly connected to the input x4 (carry = x4), and also, in an exceedingly similar approach, the approximate output add (i.e., sum) is directly connected to Fig. 5. (a) Approximate half and (b) overall structure of DQ4:2C2. Input x1 (sum = x1). Within the approximate a part of this structure, the output Cout is neglected. whereas the approximate a part of this structure is significantly quick and low power, its error rate is large (62.5%).The supplementary a part of this structure is a definite 4:2 Compressors. the structure of the projected structure is shown in Fig. 4(b). within the actual operative mode, the delay of this structure is concerning identical as that of the precise 4:2 compressors.

2) Dual Quality 4:2 compressor Structure 2 (DQ4:2C2):

within the initial structure, while ignoring Cout simplified the interior structure of the reduction stage of the multiplication, its error was massive. Within the second structure, compared with the DQ4:2C1, the output Cout is generated by connecting it on to the input x3 within the approximate half. Fig. five shows the

interior structure of the approximate half and also the overall structure of DQ4:2C2. While the error rate of this structure is that the same as that of DQ4:2C1, namely, 62.5%, its relative error is lower.

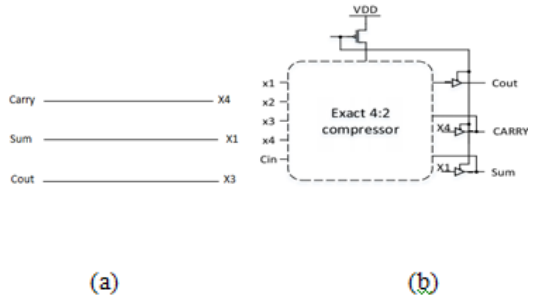



Fig.5. (a) Approximate part structure of DQ 4:2C2

(b) Overall structure of DQ 4:2C2

3) Dual Quality 4:2 compressor Structure 3 (DQ4:2C3):

The previous structures, in the approximate operative mode, had most power and delay reductions compared with those of the precise compressor . In some applications, however, a better accuracy could also be needed. Within the third structure, the accuracy of the approximate operating mode is improved by increasing the complexness of the approximate half whose internal structure is shown in Fig. 6(a). During this structure, the accuracy of output ads is inflated. The same as DQ4:2C1, the approximate a part of this structure doesn't support output Cout. The error rate of this structure, however, is reduced to five hundredth. The overall structure of DQ4:2C3 is shown in Fig. 6(b) where the supplementary half is embedded in an exceedingly red broken line rectangle. Note that during this structure, the utilized NAND gate of the approximate half (denoted by a blue line rectangle) is not used throughout the precise operative mode. Hence, during this operative mode, wepropose disconnecting provide voltage of this gate by mistreatment the power gating.

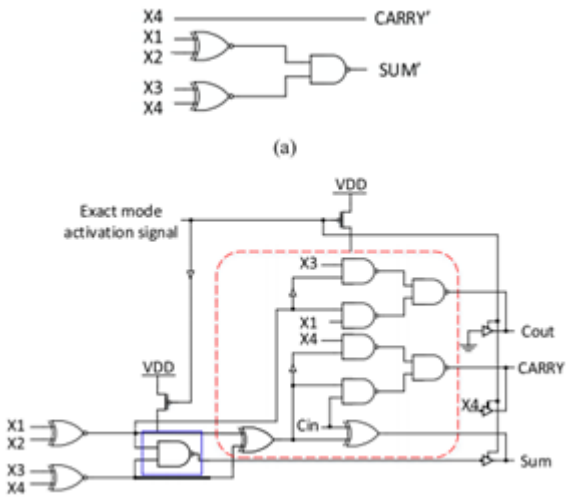



Fig. 6. (a) Approximate part of DQ4:2C3

(b) Overall structure ofDQ4:2C3

4) Dual Quality 4:2 compressor Structure 4(DQ4:2C4):

During this structure, we tend to improve the accuracy of the output carry compared there upon of DQ4:2C3 at the value of larger delay and power consumption wherever the error rate is reduced to 31.25%. The interior structure of the approximate half and therefore the overall structure of DQ4:2C4 are shown in Fig. 7. The supplementary half is indicated by red dashed line rectangular where as the gates of the approximate half, powered OFF throughout the precise Operational mode, are indicated by the blue line. Note that the error rate corresponds to the incidence of the errors within the output for the whole vary of the input. The output quality is set by the error distance (ED) parameter that is that the distinction between the precise output and the output of the approximate unit. Additionally to the impotency, there are different closely connected parameters, namely, normalized ED (NED) and mean relative impotency (MRED), that are a lot of important in crucial the output quality. Therefore, to judge the appropriateness of associate approximate unit for a mistake resilient application for a given output quality, one should consider these parameters, that are explained in Section IV.

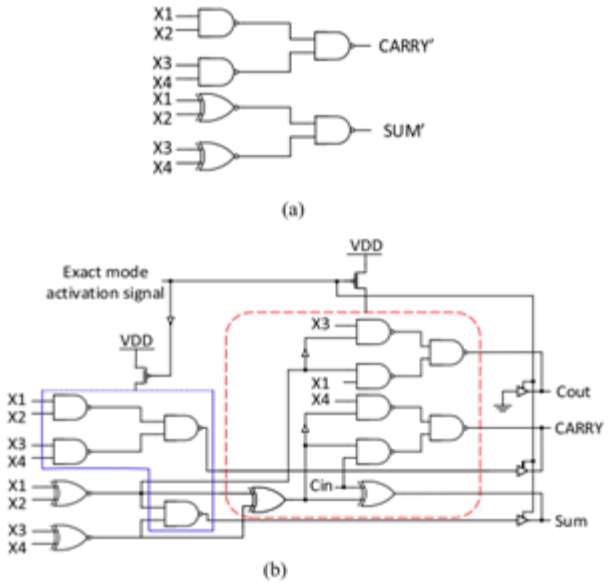



Fig.7. (a) Approximate part of DQ4:2C4

(b) Overall structure of DQ4:2C4

## 4. ACCURACY STUDY OF MULTIPLIER REALIZED BY THE PROPOSED COMPRESSORS

In this section, first the accuracy metrics considered in this paper are introduced. Next, the accuracy of 8-bit, 16-bit,32-bit Dadda multipliers accomplished by the planned compressors is studied. a correct combination of the planned compressors could also be utilized to attain a more robust exchange between the accuracy and style . Parameters .As associate choice, the use of each DQ4:2C1 and DQ4:2C4 for the LSB and MSB parts within the multiplication, severally, is usually recommended here. The results for this number are denoted by DQ4:2Cmixed. These multipliers are compared by the approximate Dadda multipliers enforced by 2 previous planned approximate 4:2 compressors mentioned in [14] in addition because the configurable number urged in [15]. Additionally, some state of-the-art approximate multiplier, that don't use approximate compressors, are thought-about. These multipliers include 32-bit unsigned ROBA (U-ROBA) [17], SSM with a section size eight (SSM8) [10], and DRUM with a section size half dozen (DRUM6) [11]. The final structure of the reduction circuitry in associate 8-bit Dadda number, that makes use of 4:2 compressors, is drawn in Fig. 7.

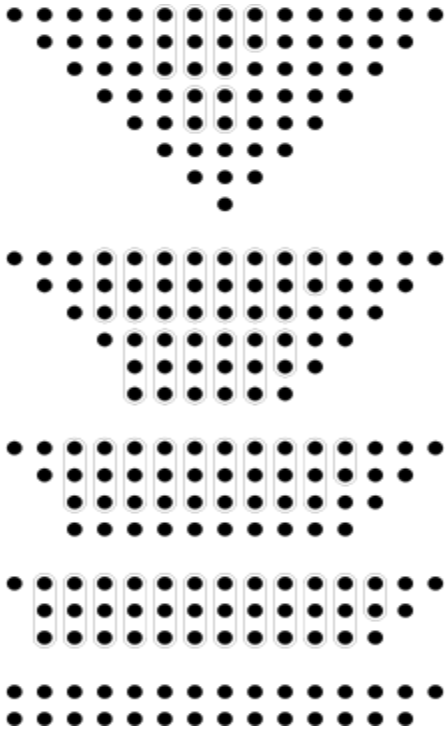


Fig. 7. Reduction circuitry of an 8-bit Dadda multiplier.

. Error Metrics

The four error metrics considered here for the accuracy evaluation include mean ED (MED), MRED, average NED, and number of the correct output. MED or mean absolute error is defined by [20]

$$\mathrm{MED} = \frac{1}{2^{2N}} \sum_{i=1}^{2^{2N}} |\mathrm{ED}_i| \qquad (4)$$

where ED*i* is the distance between the accurate and approximate output. Also, MRED, which is defined based on the calculation of the ED between the approximate and exact output for each combination of input operands divided by the exact output, is expressed by [4]

$$\mathrm{MRED} = \frac{1}{2^{2N}} \sum_{i=1}^{2^{2N}} \frac{|\mathrm{ED}_i|}{S_i}. \qquad (5)$$

In addition, in order to compare the approximate multipliers almost independent of their sizes, NED is defined as [4]

$$\mathrm{NED} = \frac{\mathrm{MED}}{D} = \frac{1}{2^{2N}} \sum_{i=1}^{2^{2N}} \frac{\mathrm{ED}_i}{D} \qquad (6)$$

where *D* is the maximum possible ED of an approximate multiplier. For most of the approximate multipliers, this value
is *(2N − 1)2*. Thus, by replacing *D* in (6) by *(2N − 1)2*, the NED may be obtained from [14]

$$\text{NED} = \frac{\text{MED}}{(2^N-1)^2} = \frac{1}{(2^N-1)^2}\sum_{i=1}^{2^{2N}}\frac{|\text{ED}_i|}{2^{2N}}. \qquad (7)$$

## 5. RESULTS AND DISCUSSION

In this section, first, the efficacies of the proposed 4:2 compressors in the approximate operating mode are investigated. In the investigation, which is performed by utilizing them in the Dadda structure, the look parameters of the multipliers are compared with those of the precise Dadda multiplier, approximate Dadda multipliers realized mistreatment the 2 approximate 4:2 compressors projected in [14], and therefore the approximate multiplier given in [15].

Next, the effectiveness of the projected compressors in their precise operational mode utilized within the Dadda multiplier can be compared therewith of the projected approximate multiplier by [15] within the same mode. Then, the performances of the approximate multipliers are assessed in some image process applications. The results of this paper & comparison of different parameters are shown below

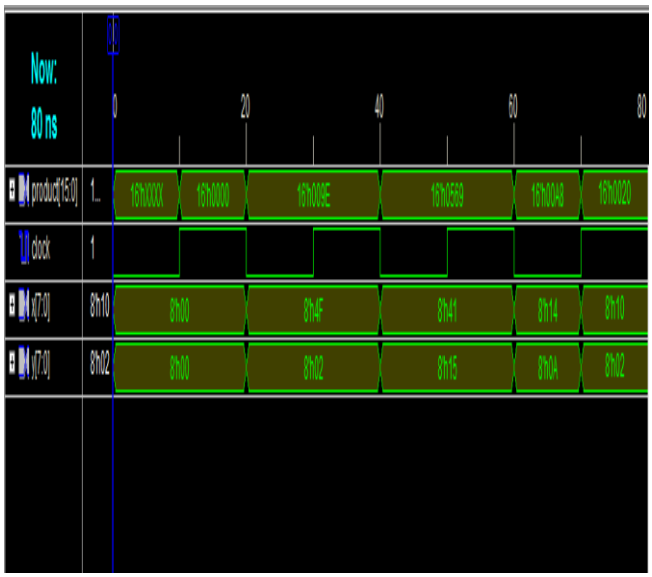



Fig. 8.Approximate Multiplier using proposed 4:2 compressors

Table: 1 Comparison of results in terms of delay, area, power

| Compressors | Delay (ns) | Area $(\mu m)^2$ | Power (µw) |
|---|---|---|---|
| **Exact** | 1.18 | 1991 | 2320 |
| **DQ4:2C1** | 0.48 | 326 | 154 |
| **DQ4:2C2** | 0.52 | 344 | 169 |
| **DQ4:2C3** | 0.69 | 336 | 651 |
| **DQ4:2C4** | 0.77 | 1174 | 841 |
| **DQ4:2Cmixed** | 0.68 | 765 | 519 |

### 1.Image process Applications

In this section, to assess the effectiveness of the planned compressors in real applications, they're used in 3 image process applications. Here, we tend to used six 8-bit approximate multipliers architectures along with the 2 compressors planned in [14]. The three studied image process applications were smoothing, sharpening, and image multiplication. all told the thought-about image processing applications, the output image qualities obtained by employing the multipliers of [15], SSM8, and DRUM6 were larger than 0.9, that is extremely near one because the price for the perfect quality, and hence, their results haven't been according here. In the sharpening application [15], the output sharpened image is obtained from

$$Y(i,j) = 2.X(i+m, j+n) - \frac{1}{273}\sum_{m=-2}^{2}\sum_{n=-2}^{2} \times X(i+m, j+n)\cdot \text{Mask}_{\text{Sharpening},1}(m+3, n+3) \qquad (8)$$

where X and Y are the input and output images, and Mask Sharpening matrix is

$$\text{Mask}_{\text{sharpening}} = \begin{bmatrix} 1 & 4 & 7 & 4 & 1 \\ 4 & 16 & 26 & 16 & 4 \\ 7 & 26 & 41 & 26 & 7 \\ 4 & 16 & 26 & 16 & 4 \\ 1 & 4 & 7 & 4 & 1 \end{bmatrix}. \qquad (9)$$

For the smoothing application, the following equation is used to determine the smoothed output image:

$$Y(i,j) = \frac{1}{60}\sum_{m=-2}^{2}\sum_{n=-2}^{2} \times X(i+m, j+n)\cdot \text{Mask}(m+3, n+3) \qquad (10)$$

where Mask Smoothing is given by

$$\text{Mask}_{\text{smoothing}} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & 4 & 4 & 4 & 1 \\ 1 & 4 & 12 & 4 & 1 \\ 1 & 4 & 4 & 4 & 1 \\ 1 & 4 & 7 & 4 & 1 \end{bmatrix}. \qquad (11)$$

A more robust parameter for this purpose is mean structural similarity index metric (MSSIM), that works supported measuring the structural similarity of the precise and approximate pictures

## 6. CONCLUSION

In this project, we have a tendency to propose four DQ4:2Cs that had the flexibility of change between the precise and approximate operating modes. Within the approximate mode, these compressors provided higher speeds and lower power consumptions at the cost of lower accuracy. Every of those compressors had its own level of accuracy within the approximate mode moreover as different delays and powers within the approximate and precise modes. These compressors were utilized within the structure of a 32-bit Dadda multiplier to supply a configurable multiplier whose accuracy (as well as its power and speed) may be changed dynamically throughout the runtime. Our studies disclosed that for the 32-bit multiplication, the projected compressors yielded, on average, forty sixth and sixty eight lower delay and power consumption within the approximate mode compared with those of the recently urged approximate compressors. Also, utilizing the projected compressors in 32-bit Dadda multiplier provided, on average, regarding thirty third lower NED compared with the progressive compressor-based approximate multipliers. When examination with no compressor-based approximate multipliers, the errors of the projected multipliers were higher while the look parameters were significantly higher. Finally our studies showed that the multipliers accomplished supported the urged compressors have, on average, about 93% smaller FOM price compared with the thought-about approximate multiplier.

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